REMARKS

An Excess Claim Fee Payment Letter is attached hereto to cover the cost of the excess claims added by this Amendment.

Claims 15-39 are all the claims presently pending in the application. Claims 16-17, 20-22, 25, 28-29, and 33 have been amended to more particularly define the invention. Claims 37-39 have been added to claim additional features of the claimed inevntion. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant gratefully acknowledges the Examiner's indication that claims 23-26 and 34-35 would be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable and, therefore, declines to rewrite the claims at this time.

Claims 15-22, 27-33, and 36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Chan, et al. (U.S. Patent No. 6,140,684).

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as recited, for example, in claim 15) is directed to a method of forming an N-channel metal oxide semiconductor (NMOS) driver circuit. The method includes forming a boost gate stack on a substrate, the boost gate stack having a source and drain formed by a low concentration N-type implantation, and coupling an N-driver to the boost gate stack.

Conventional methods use a high dopant level to form an NMOS driver circuit. However, such a high dopant level causes an array to have leakage (Application at page 13,

lines 1-4).

The claimed NMOS driver circuit, on the other hand, includes a boost gate stack having a source and drain formed by a low concentration (e.g.,. less than about 1 x 10^{14} ions per cm^3) N-type implantation (Application at page 6, lines 17-20). This allows the claimed NMOS driver circuit to minimize leakage (Application at page 13, lines 4-12).

II. THE CHAN REFERENCE

The Examiner alleges that Chan teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Chan.

Chan discloses a static random access memory (SRAM) cell having two bulk silicon pull-down transistors of a first conductivity type, two active gated pull-up thin-film transistors (TFTs) of a second conductivity type, two pass gates, a common word line, and two bit line contacts. The bulk silicon pull-down transistors, two active gated pull up TFTs, and two pass gates are connected at four shared contacts. In addition, the two bulk silicon pull-down transistors and the two active gated pull-up TFTs are formed with two polysilicon layers, a first of the polysilicon layers (poly1) is salicided and includes poly1 gate electrodes for the two bulk silicon pull-down transistors (Chan at Abstract)..

However, Applicant respectfully submits that Chan does not teach or suggest an NMOS driver circuit with a boost gate stack having a source and drain *"formed by a low concentration N-type implantation"*, as recited, for example, in claims 15, 29 and 31. As noted above, conventional methods use a high dopant level to form an NMOS driver circuit. However, such a high dopant level causes an array to have leakage (Application at page 13, lines 1-4).

The claimed NMOS driver circuit, on the other hand, includes a boost gate stack having a source and drain formed by a low concentration N-type implantation (Application at page 6, lines 17-20). For example, the low concentration N-type implantation may include no more that about 1 x 1014 dopant ions per cm3 (Application at page 11, lines 10-14; Figure 2A). This allows the claimed NMOS driver circuit to minimize leakage (Application at page

13, lines 4-12).

Clearly, these novel features are not taught or suggested by Chan. Indeed, Chan clearly does not teach or suggest a low concentration N-type implantation as in the claimed invention. In fact, the Examiner completely fails to address the lack of this feature in Chan. Indeed, the Examiner concedes that source/drain regions in Chan "are manufactured by methods known in the art" (Office Action at page 3, second paragraph). As explained in the Application, the present invention clearly differs from conventional processes (Application at page 13, lines 1-3).

The Examiner attempts to rely on the passage at col. 5, lines 4-18 in Chan to support his allegations. Specifically, the Examiner attempts to equate the source/drain regions 60 illustrated in Figure 3 of Chan, with the source and drain regions of the claimed invention. However, this clearly not the case.

Indeed, this passage of Chan merely states that "source/drain regions 60 are formed for the N-channel transistors 16 and 20 by methods known in the art" and that these regions are "typically implanted with an N+ type dopant such as arsenic or phosphorus" (Chan at col. 5, lines 7-18). Thus, nowhere does this passage teach or suggest a low concentration N-type implantation.

In fact, nowhere does Chan teach or suggest a low concentration N-type implantation as in the claimed invention. Indeed, the level of implantation in forming source/drain regions are completely irrelevant in Chan. Thus, the Chan method is completely unrelated to the claimed invention, as evident from the manufacturing processes outlined in Chan (Chan at col. 7, line 19-col. 8, line 38).

Therefore, contrary to the Examiner's allegations, Chan does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 15-39, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in

condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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